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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

042054

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on _____

Signature _____

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name _____

Application Number

10/767,167

Filed

January 30, 2004

First Named Inventor

Akira MIURA

Art Unit

2893

Examiner

Matthew L. Reames

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐

applicant/inventor.

☐

assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)☒

attorney or agent of record.

Registration number 59145

☐

attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 _____



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Telephone number

April 1, 2009

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒

*Total of 1 forms are submitted.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Akira MIURA et al.**

Art Unit: **2893**

Application Number: **10/767,167**

Examiner: **Matthew L. Reames**

Filed: **January 30, 2004**

Confirmation Number: **4743**

For: **INTEGRATED CIRCUIT**

Attorney Docket Number: **042054**

Customer Number: **38834**

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop: AF

Date: April 1, 2009

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

Sir:

This Request is filed concurrent with a Notice of Appeal in compliance with 37 C.F.R. §41.31. Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

REMARKS

Claims 1, 2 and 3-14 are pending in the application. Claims 1, 2 and 4-13 stand rejected.

Claim Rejections - 35 U.S.C. § 103(a):

Claims 1, 2, 5-8 and 11-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Mori et al.* (US Patent 5,247,223), hereinafter referred to as *Mori*.

Regarding the newly added feature of a magnetic field generating unit (of claim 1), the Examiner contends that it is disclosed in *Mori* in column 6, lines 54-58. Here *Mori* discloses:

However, for example, if a magnetic field is applied in the direction perpendicular to the paper surface in FIG. 2 the phases of electron waves can be also changed by the magnetic field.

As such, the Examiner contends that a magnetic field generating unit is disclosed. However, the Examiner's position is incorrect for the following reasons.

First, claim 1 recites that a magnetic field generating unit is comprised *in an integrated circuit*. *Mori* does not disclose or fairly suggest this feature. As shown in FIG. 2 of *Mori* (which the above recited passage discusses), the structure appears to be an experimental implementation. It is quite evident that the structure is **not** an integrated circuit as recited in claim 1 of the present application. *Mori* itself, when referring to FIG. 3 states that it is a practical structure of an AB effect transistor, as opposed to FIG. 2 which appears to be an experimental configuration which is **not** an integrated circuit.

Second, a magnetic field is disclosed in *Mori*, not a magnetic field generating unit, as recited in claim 1. *Mori* does not disclose or suggest a magnetic field generating unit. As will be discussed regarding claims 12 and 13, the magnetic field generating unit is further defined to be either coils or two current lines. No indication of how a magnetic field is generated is discussed in *Mori*.

Third, the above recited passage applies to FIG. 2 of *Mori*. This is a different embodiment than shown and described by FIG. 3, which the Examiner uses to reject claim 1. Thus, *Mori* does not appear to disclose using a magnetic field with the device as shown in FIG. 3. As such, the Examiner must provide a rationale for combining the two embodiments, which has not been done.

However, such a rationale does not exist. The device as shown in FIG. 3 of *Mori* appears to use a gate voltage, not a magnetic field, to influence the electrons. As recited in column 4, lines 5-10 (discussing FIG. 3):

When the device is actually used, one of the gate electrodes G₁ and G₂ for example, the gate electrode G₂ is connected to the ground and the gate voltage which is applied to the gate electrode G₁ is changed.

Thus, it appears from the recited passage that an *electric field* is used, [i.e. produced by a gate voltage] to influence the electrons. That is, the entire structure as shown in FIG. 3 of *Mori* appears directed at creating an electric field, not a magnetic one. *Mori* does not suggest using a magnetic field generating device in the embodiment shown in FIG. 3. To the contrary, as recited above, *Mori* appears to show using an electric field, vis a vis the gate voltage. *Mori* only appears to disclose using a magnetic field in the device shown in FIG. 2. Using an electric field (as apparently taught in FIG. 3) with a magnetic field (as discussed in FIG. 2) would be redundant and would not be implemented by a person having ordinary skill in the art.

Dependent Claim 5:

The Examiner contends that integrated optical devices with transistors and optical devices was well known in the art. The Examiner provides no support for his contention and as such, does not satisfy his burden of showing a prima facie case of obviousness.

Dependent Claim 7:

Claim 7 recites that a thermionic cathode is used as a cathode of the vacuum element. The Examiner insists that a “cold cathode,” as recited in *Mori*, discloses the thermionic cathode of claim 7. The examiner provides no support for this contention. Applicants have disputed the examiner’s assertion and maintain that a cold cathode does not disclose a thermionic cathode. The examiner must present some evidence as to why he believes a cold cathode discloses a thermionic cathode. According to MPEP 2144.03(C):

If applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the examiner must support the finding with adequate evidence.

In the absence of any evidence, the examiner has not met his burden of showing a prima facie case of obviousness.

Dependent Claim 8:

Dependent claim 8 recites that a carbon nanotube is attached to the thermionic cathode. The examiner contends that this feature is “well known in the art,” but provides no evidence to support his position. Applicants have disputed this statement in previous correspondence with the examiner. The examiner must provide some evidence to support his position by showing the feature in a prior art reference and providing a reason to combine the respective references to arrive at the claimed invention.¹ In the absence of this, the examiner has not met his burden of showing prima facie obviousness.

Dependent Claims 12 and 13:

Dependent claims 12 and 13 recite that said magnetic field generating unit is a coil or two current lines, respectively. The Examiner contends that these features would be obvious and are conventional methods of generating a magnetic field. The examiner provides no support for his position. As indicated above, the examiner must provide some evidence to support his position. Without such evidence, the examiner has not met his prima facie burden of showing obviousness.

Claims 1, 2, 4 and 9-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Okada* (US Patent 5,003,360) in view of *Mori*.

Regarding the newly added feature of a magnetic field generating unit, similar arguments mentioned above also apply to this rejection. That is, *Okada* does appear to disclose a magnetic field in column 3, line 7. However, as mentioned above with respect to *Mori*, *Okada* does not disclose a magnetic field generating unit located in an integrated circuit.

The above referenced magnetic field is mentioned with respect to FIG. 1 of *Okada*. However, as shown in FIG. 1, it is **not** an integrated circuit. FIG. 1 is described as a:

¹ MPEP 2144.03(C).

schematic illustration of a quantum interference effect element model for explaining a quantum interference effect.

Thus, FIG. 1 of *Okada* does not disclose an integrated circuit. Thus, a required element of claim 1 is not disclosed or fairly suggested by the cited references.

CONCLUSION

In light of the aforementioned remarks, applicants respectfully submit that the rejection is improper and ask that the application be place in condition for allowance.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

A handwritten signature in black ink, appearing to read 'D. Hubbs', is written over the printed name.

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